

FIG. 1

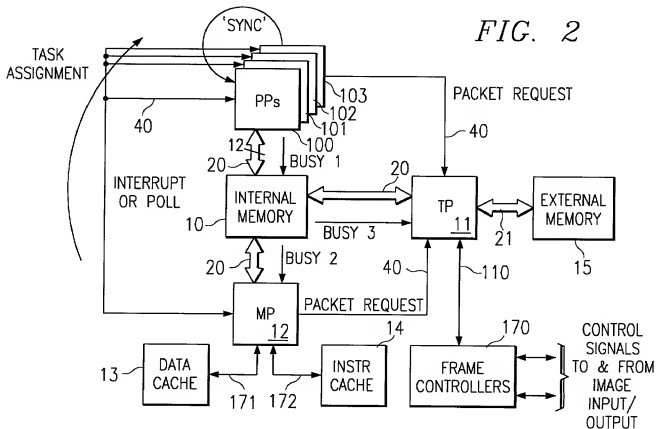


FIG. 2

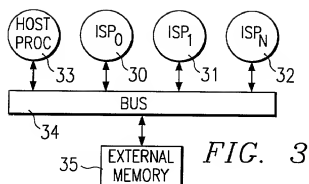


FIG. 3

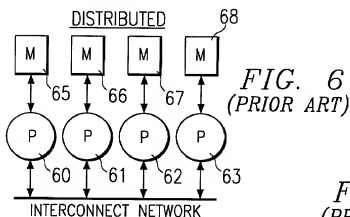
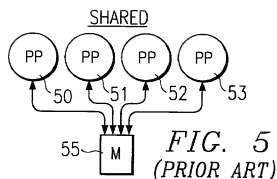
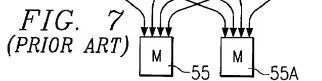
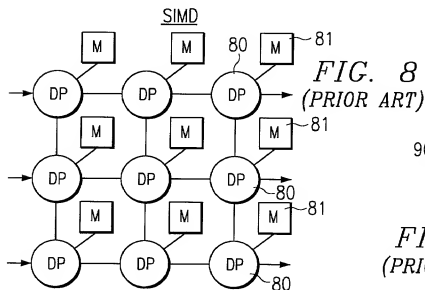
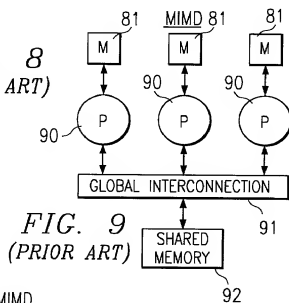
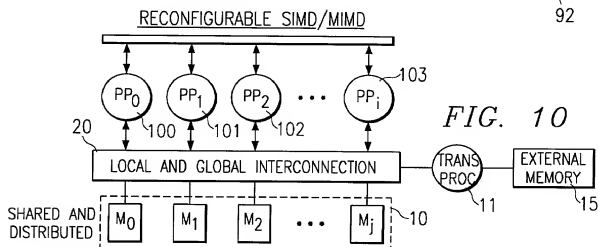
FIG. 6
(PRIOR ART)FIG. 5
(PRIOR ART)FIG. 7
(PRIOR ART)FIG. 8
(PRIOR ART)FIG. 9
(PRIOR ART)

FIG. 10

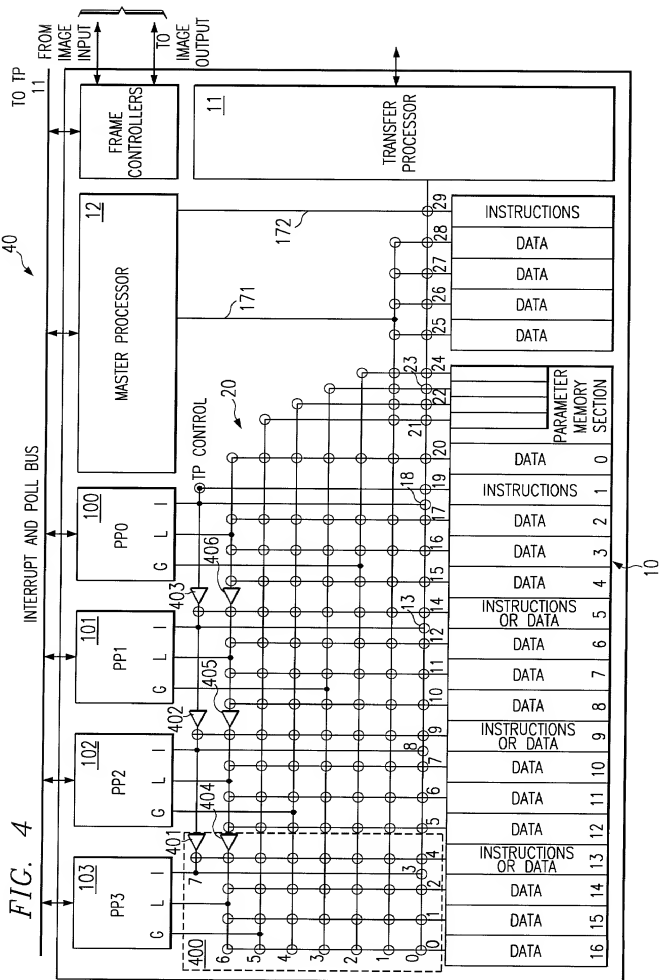


FIG. 11

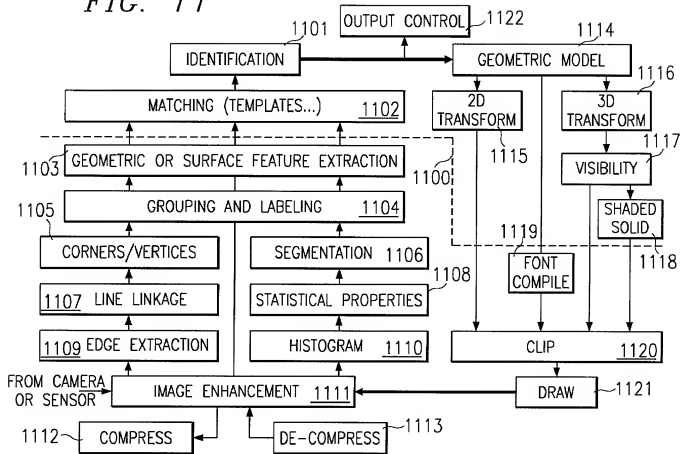


FIG. 12

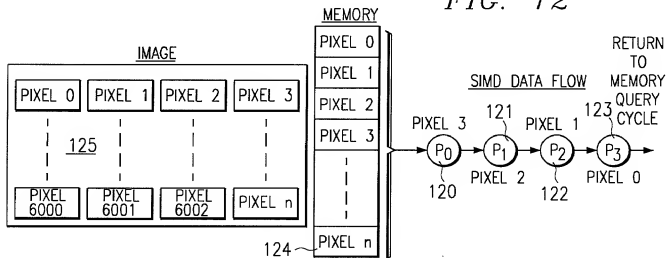


FIG. 13

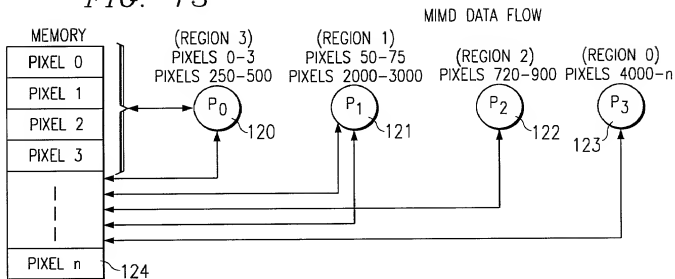


FIG. 14

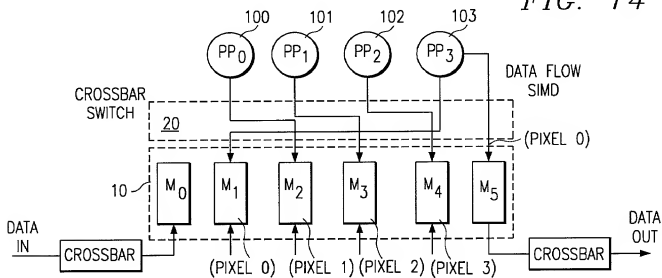


FIG. 15

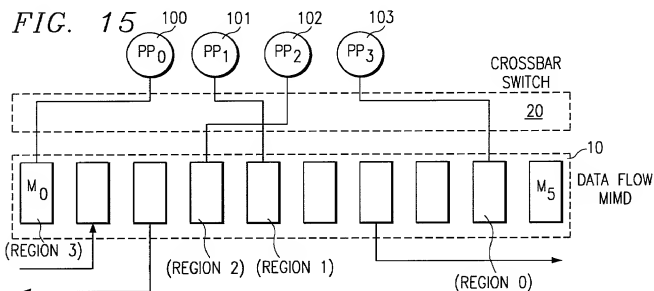


FIG. 16

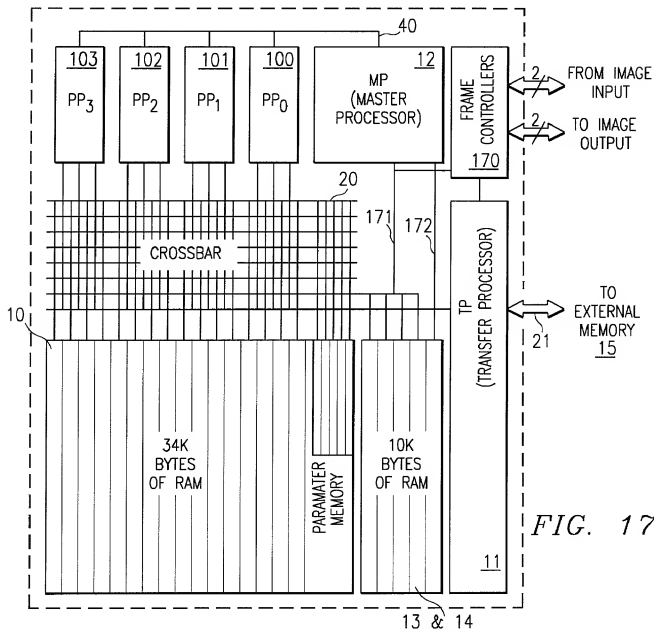
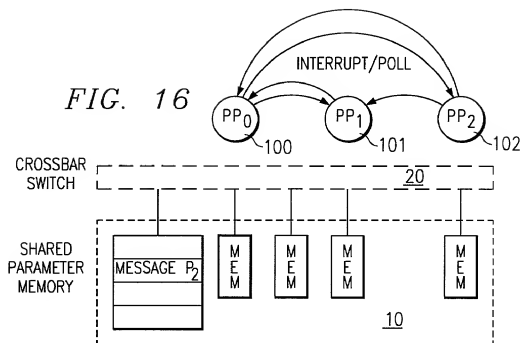


FIG. 17

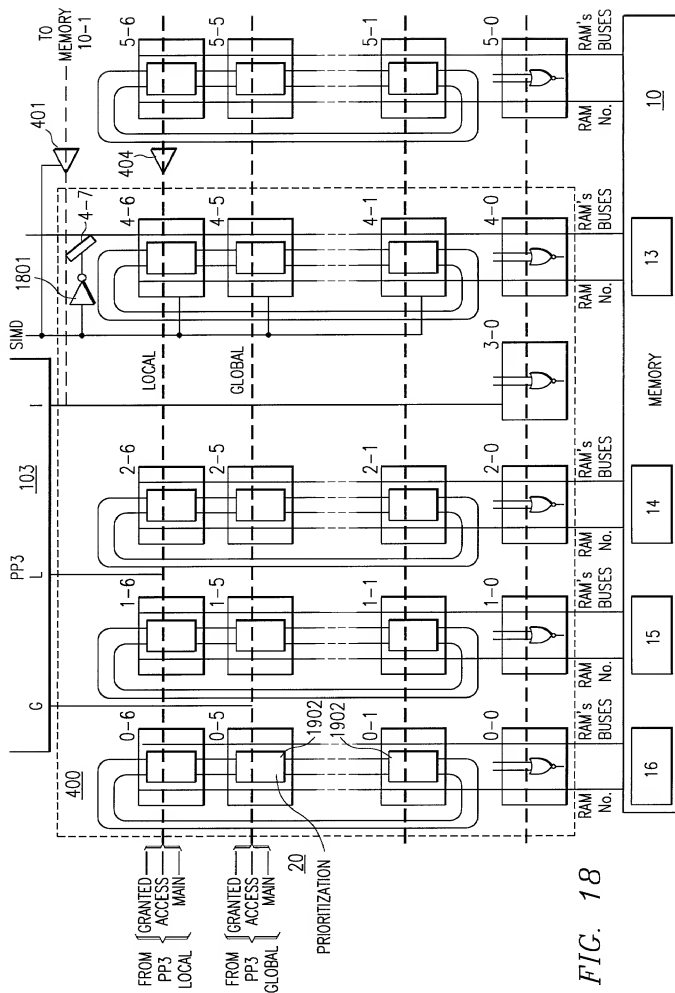


FIG. 18

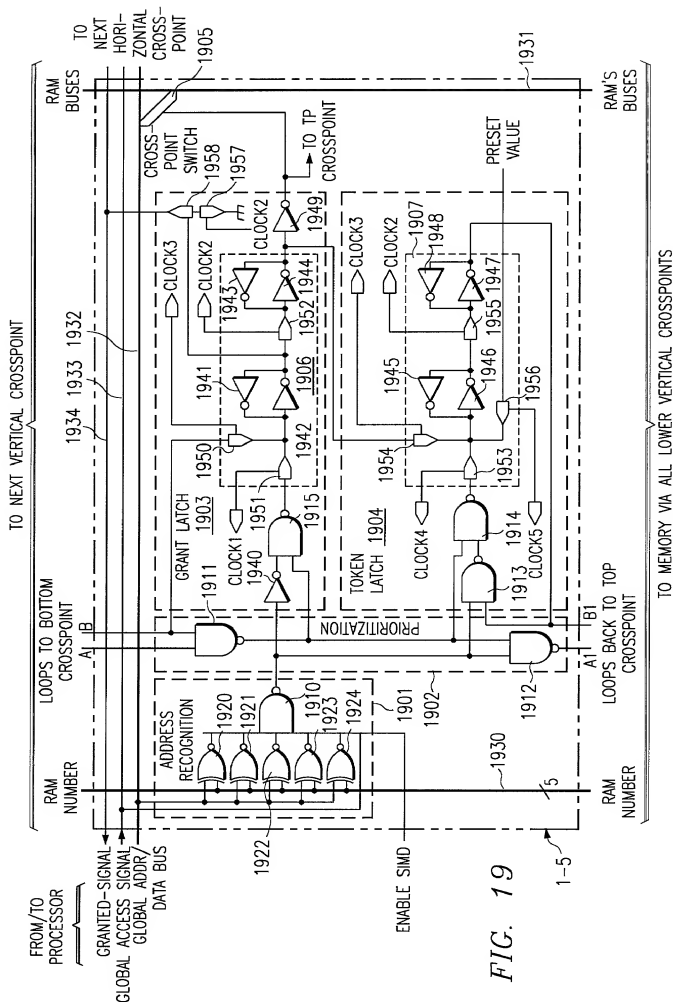
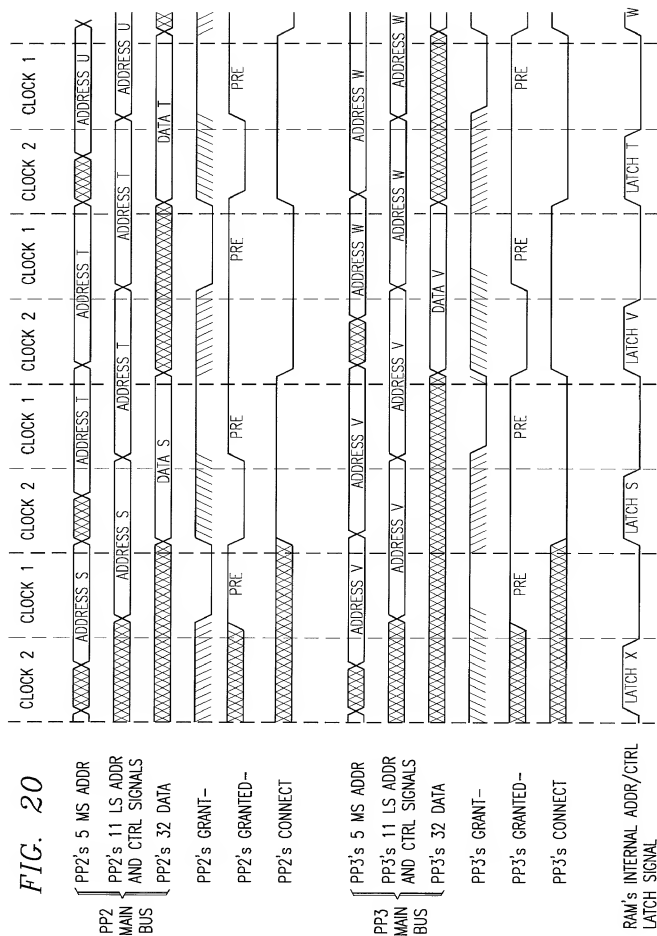


FIG. 20



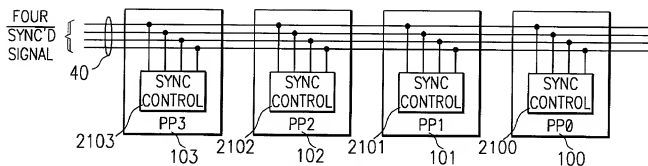


FIG. 21

>0000	>0800	>1000	>1800	>2000	>2800	>3000	>3800
64 PIXELS	64 PIXELS	64 PIXELS	>1900 >193F	>2100 >213F	64 PIXELS	64 PIXELS	64 PIXELS
			>1940				
>07FF	>0FFF	>17FF	>1FFF	>27FF	>2FFF	>37FF	>3FFF
0	1	2	3	4	5	6	7

$$\begin{array}{l}
 \text{NORMAL ARITHMETIC} \left\{ \begin{array}{l}
 >193F - 0001100100111111 \\
 + \\
 >0001 - 0000000000000001 \\
 = \\
 >1940 - 0001100101000000
 \end{array} \right.
 \end{array}$$

$$\begin{array}{l}
 \text{SLICED ARITHMETIC} \left\{ \begin{array}{l}
 >193F - 0001100100111111 \\
 \text{(SLICE MASK)} \quad 0000 \overbrace{1111100000}^{\text{SLICE NUMBER}} \\
 + \\
 >0001 - 0000000000000001 \\
 = \\
 >2100 - 0010000100000000
 \end{array} \right.
 \end{array}$$

CARRY

FIG. 22

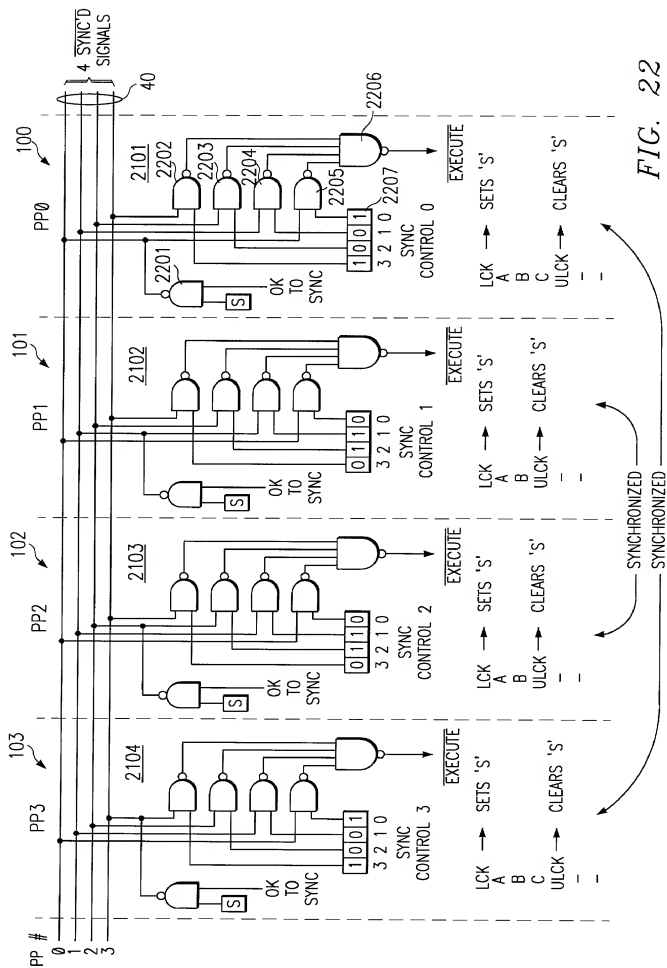


FIG. 22

FIG. 23

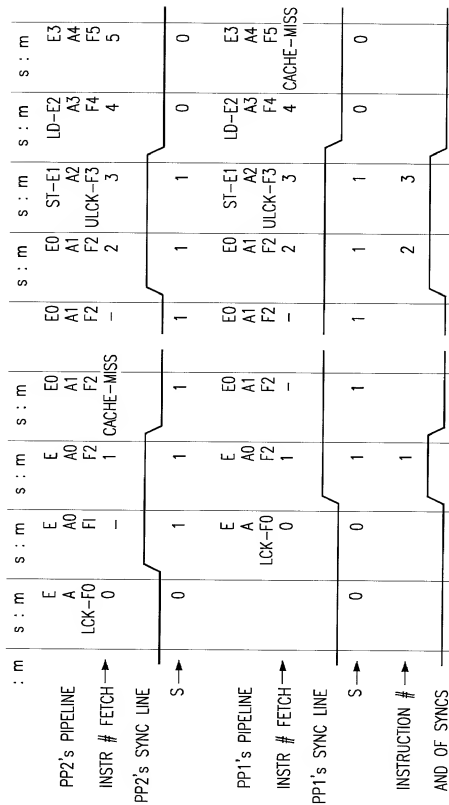
FIG. 23

	<u>PP2:</u>		<u>PP1:</u>	
	0	LCK	0	LCK
	1	ST *A0,D0	1	ST *A1,D0
	2	LD *A1,D0	2	LD *A0,D0
	3	ULCK	3	ULCK
	4	—	4	—
	5	—	5	—

(3210)
 SYNC BITS = 0110
 IN BOTH PP2 AND PP1

m — MASTER CLOCK
 s — SLAVE CLOCK

m - MASTER CLOCK
s - SLAVE CLOCK



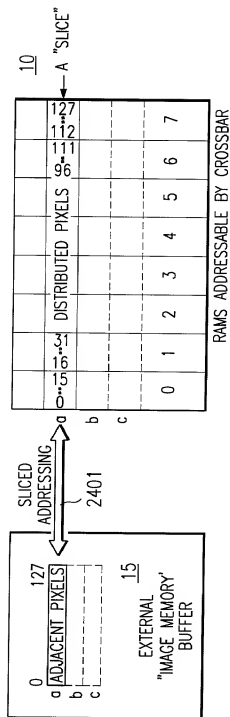


FIG. 24

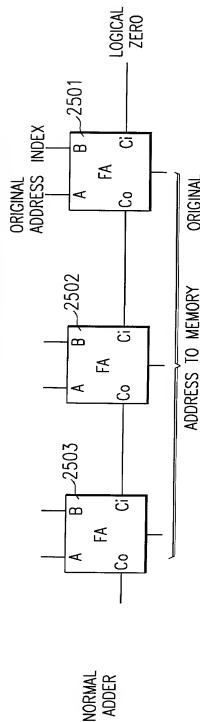


FIG. 25
(PRIOR ART)

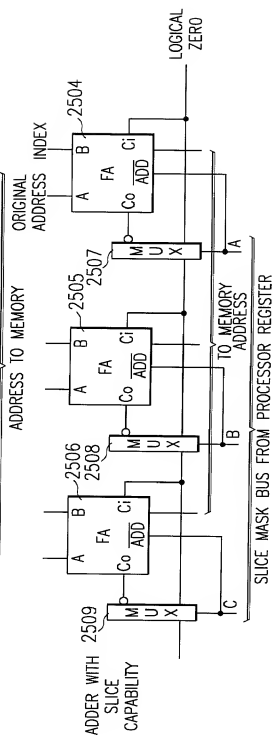
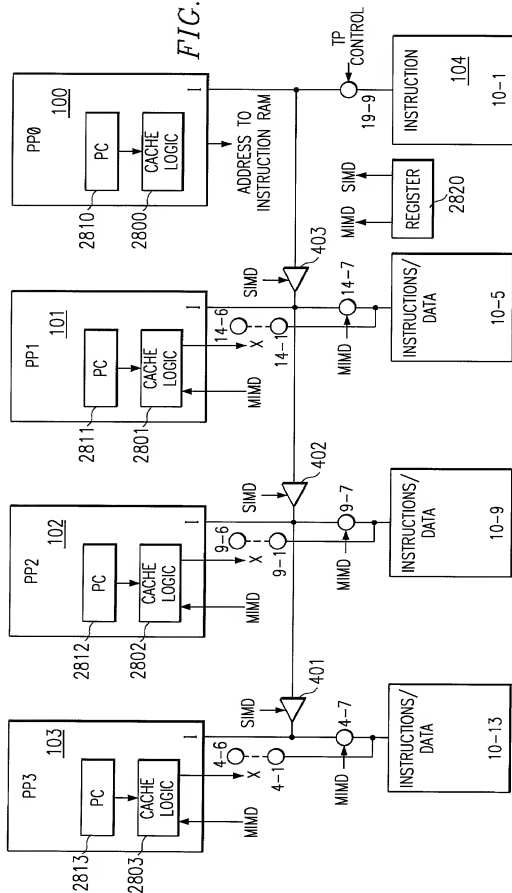


FIG. 26

FIG. 28



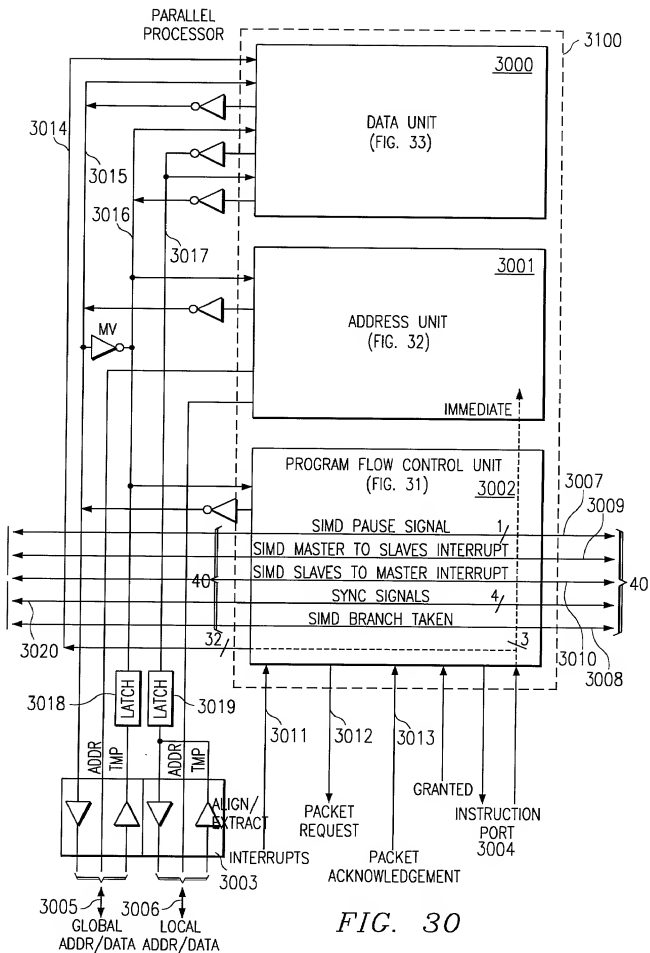


FIG. 30

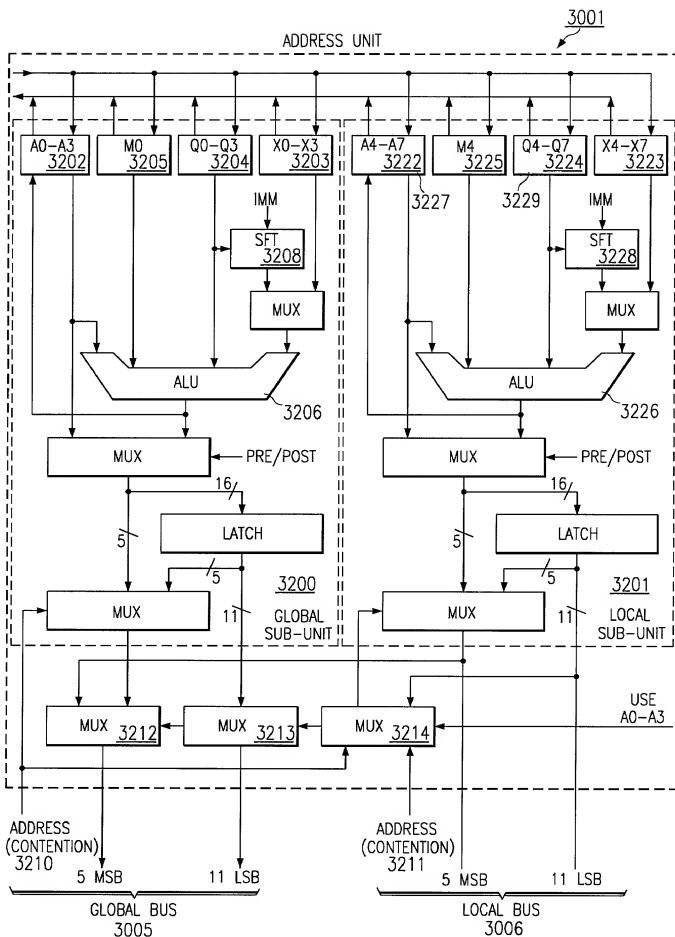
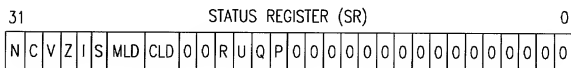
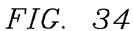
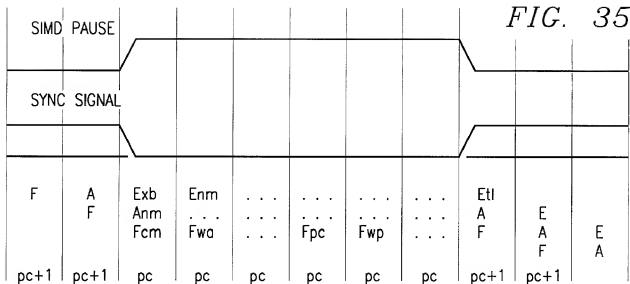


FIG. 32

3000





Fcm - CACHE-MISS

Anm - NO MASTER PHASE OF THE ADDRESS UNIT, THUS NO REGISTER MODIFY.

Exb - CROSSBAR ACCESS(ES) OCCUR. STORES COMPLETE TO MEMORY. LOADS COMPLETE INTO TEMPORARY LATCHES, MASTER PHASE OF DATA UNIT OPERATIONS KILLED.

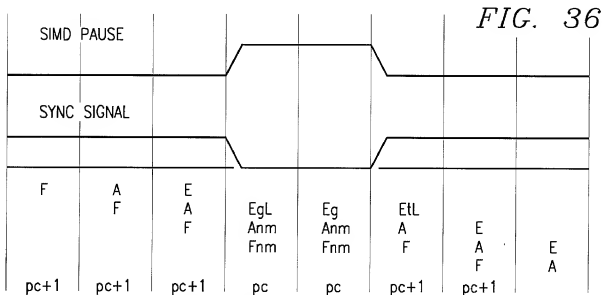
Enm - NO MASTER PHASE OF DATA UNIT.

Fwa - WAIT FOR CACHE-MISS ACKNOWLEDGE FROM TP.

Fpc - TRANSFER PC AND SEGMENT NUMBER TO TP

Fwp - WAIT FOR SUBSEGMENT PRESENT FLAG TO BECOME SET.

EtI - TEMPORARY LATCH DATA (LOADS) COMPLETE INTO DESIGNATION REGISTER(S). DATA UNIT PERFORMS ITS ALU/MPY OPERATIONS.



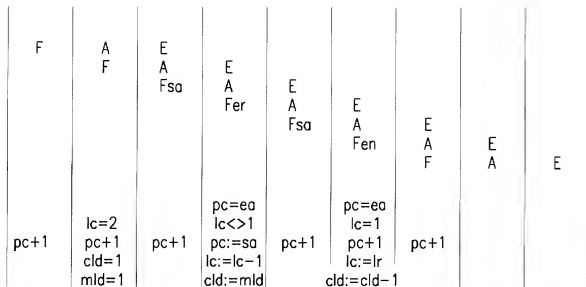
EgI - CONTENTION DETECTED ON BOTH GLOBAL AND LOCAL BUSES. NO MASTER PHASE IN DATA UNIT.

Fnm - NO MASTER PHASE ON FETCH. PIPE NOT LOADED.

Eg - CONTENTION DETECTED ON GLOBAL BUS. LOCAL BUS TRANSFER OCCURS. STORE TO MEMORY, OR LOAD TO TEMP REGISTER. NO MASTER PHASE IN DATA UNIT.

EtI - TEMPORARY LATCH DATA (LOADS) COMPLETE INTO DESTINATION REGISTER(S). DATA UNIT PERFORMS ITS ALU/MPY OPERATIONS.

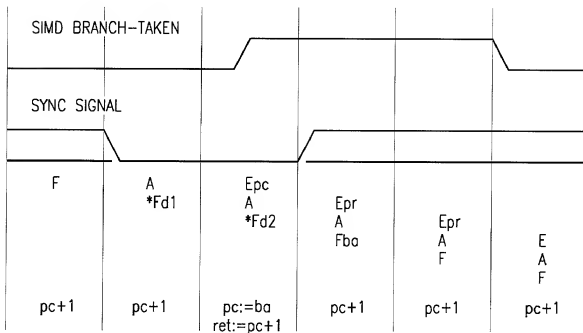
Anm - NO MASTER PHASE IN ADDRESS UNIT. ADDRESS REGISTER NOT MODIFIED.



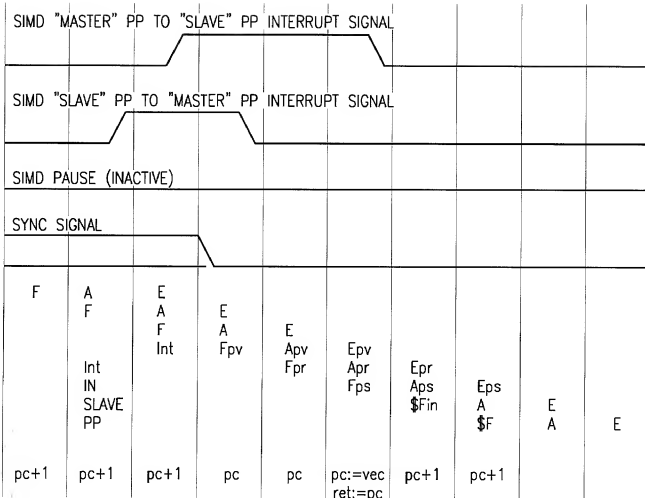
Fsa - START ADDRESS OF LOOP. PC INCREMENTS NORMALLY.
 Fer - END ADDRESS, REPEAT LOOP. LOOP COUNTER NOT ONE. LOAD PC WITH START ADD.
 Fen - END ADDRESS, NO-REPETITION. LOOP COUNTER IS ONE. PC INCREMENTS NORMALLY.

FIG. 37

FIG. 38



Epc - COPY PC+1 INTO RET. LOAD PC WITH BRANCH ADDRESS.
 Epr - PUSH RET IF A CALL. (EITHER Epr CAN PUSH THE RETURN ADDRESS).
 Fd1 - DELAY SLOT 1 INSTRUCTION FETCH.
 Fd2 - DELAY SLOT 2 INSTRUCTION FETCH.
 Fba - FETCH INSTRUCTION FROM BRANCH ADDRESS.
 * - INTERRUPTS LOCKED OUT.



Int - INTERRUPT OCCURS.

Fpv - PSEUDO INSTRUCTION. (PC TO RET. VECTOR FETCH INTO PC).

Apv - CALCULATE INTERRUPT VECTOR ADDRESS.

Epv - COPY PC TO RET. FETCH INTERRUPT VECTOR INTO PC.

Fpr - PSEUDO INSTRUCTION. (PUSH RET).

Apr - CALCULATE STACK PUSH ADDRESS.

Epr - PUSH RET ONTO STACK.

Fps - PSEUDO INSTRUCTION. (PUSH SR).

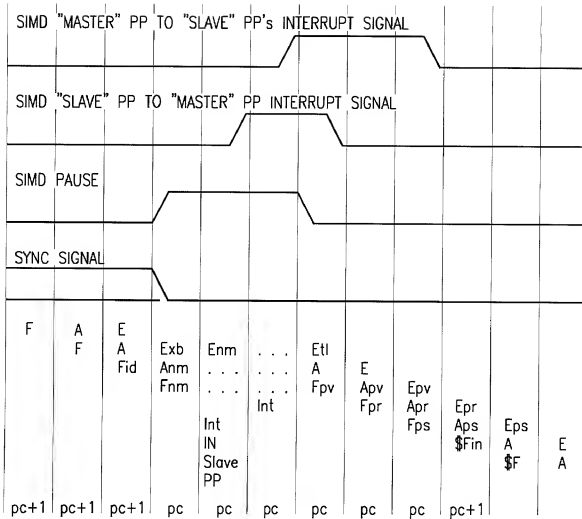
Aps - CALCULATE STACK PUSH ADDRESS.

Eps - PUSH SR ONTO STACK. CLEAR S, I AND CLD BITS IN SR.

Fin - FIRST INSTRUCTION OF INTERRUPT ROUTINE.

\$ - SYNC, INTERRUPTS AND LOOPING DISABLED UNTIL AFTER SR HAS BEEN PUSHED.
NEITHER OF FIRST TWO INSTRUCTIONS OF INTERRUPT ROUTINE MAY BE A LCK.

FIG. 39



Fid - IDLE INSTRUCTION FETCHED.

Fnm - NO MASTER PHASE ON INSTRUCTION FETCH. PIPELINE NOT LOADED.

Anm - NO MASTER PHASE ON INSTRUCTION FETCH. ADDRESS REGISTERS NOT MODIFIED.

Exb - CROSSBAR ACCESS(ES) OCCUR. STORES COMPLETE TO MEMORY. LOADS COMPLETE INTO TEMPORARY LATCHES. MASTER PHASE OF DATA UNIT OPERATIONS KILLED.

Enm - NO MASTER PHASE IN DATA UNIT.

Int - INTERRUPT OCCURS.

Etl - TEMPORARY LATCH DATA (LOADS) COMPLETE INTO DESTINATION REGISTER(S). DATA UNIT PERFORMS ITS ALU/MPY OPERATIONS.

Fpv - PSEUDO INSTRUCTION. (PC TO RET. VECTOR FETCH INTO PC).

Apv - CALCULATE INTERRUPT VECTOR ADDRESS.

Epv - COPY PC TO RET. FETCH INTERRUPT VECTOR INTO PC.

Fpr - PSEUDO INSTRUCTION. (PUSH RET).

Apr - CALCULATE STACK PUSH ADDRESS.

Epr - PUSH RET ONTO STACK.

Fps - PSEUDO INSTRUCTION. (PUSH SR).

Aps - CALCULATE STACK PUSH ADDRESS.

Eps - PUSH SR ONTO STACK. CLEAR S, I AND CLD BITS IN SR.

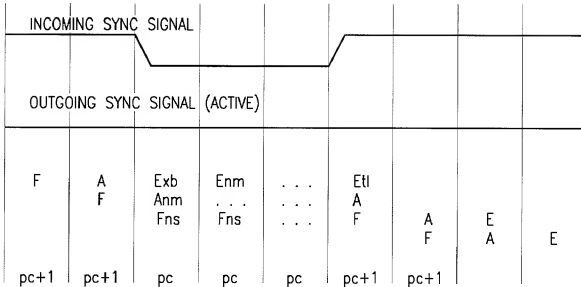
Fin - FIRST INSTRUCTION OF INTERRUPT ROUTINE.

\$ - SYNC, INTERRUPTS AND LOOPING DISABLED UNTIL AFTER SR HAS BEEN PUSHED. NEITHER OF FIRST TWO INSTRUCTIONS OF INTERRUPT ROUTINE MAY BE A LCK.

FIG. 40

00075136-060601

FIG. 41



Fns - NO SYNC CONDITION. PIPE NOT LOADED. PC UNALTERED.

Anm - NO MASTER PHASE IN ADDRESS UNIT. ADDRESS REGISTERS NOT MODIFIED.

Exb - CROSSBAR ACCESS(ES) OCCUR. STORES COMPLETE TO MEMORY. LOADS COMPLETE INTO TEMPORARY LATCHES. MASTER PHASE OF DATA UNIT OPERATIONS KILLED.

Enm - NO MASTER PHASE IN DATA UNIT.

ETL - TEMPORARY LATCH DATA (LOADS) COMPLETE INTO DESIGNATION REGISTER(S).
DATA UNIT PERFORMS ITS ALU/MPY OPERATIONS.

FIG. 42

LOADS: (ASSUMING NO SIGN-EXTENSION)

		BYTE NO.	
SOURCE DATA:		3 2 1 0	
		- - - -	
0000h =	D C B A		(MEMORY)
0004h =	H G F E		
DESTINATION =	? ? ? ?		(REGISTER)

16-BIT				32-BIT			
OP.	ADD.	LOADS...	REG VALUE	OP.	ADD.	LOADS...	REG VALUE
LD	0000h	0 0 B A	0 0 B A	LD	0000h	D C B A	D C B A
LDU	0002h	- - - -	0 0 B A	LDU	0004h	- - - -	D C B A
LD	0001h	- - - B	? ? ? B	LD	0001h	- D C B	? D C B
LDU	0003h	0 0 C -	0 0 C B	LDU	0005h	E - - -	E D C B
LD	0002h	0 0 D C	0 0 D C	LD	0002h	- - D C	? ? D C
LDU	0004h	- - - -	0 0 D C	LDU	0006h	F E - -	F E D C
LD	0003h	- - - D	? ? ? D	LD	0003h	- - - D	? ? ? D
LDU	0005h	0 0 E -	0 0 E D	LDU	0007h	G F E -	G F E D

STORES:

SOURCE DATA: = D C B A (REGISTER)

DESTINATION DATA: =
BYTE NO.
3 2 1 00000h = ? ? ? ? (MEMORY)
0004h = ? ? ? ?

OP.	ADD.	16-BIT	0000h	OP.	ADD.	32-BIT	REG VALUE
		STORES...	0004h			STORES...	
ST	0000h	0 0 B A	? ? B A ? ? ? ?	ST	0000h	D C B A	D C B A ? ? ? ?
STU	0002h	- - - -	? ? B A ? ? ? ?	STU	0004h	- - - -	D C B A ? ? ? ?
ST	0001h	- - A -	? ? A ? ? ? ? ?	ST	0001h	C B A -	C B A ? ? ? ? ?
STU	0003h	- B - -	? B A ? ? ? ? ?	STU	0005h	- - - D	C B A ? ? ? ? D
ST	0002h	- A - -	? A ? ? ? ? ? ?	ST	0002h	B A - -	B A ? ? ? ? ? ?
STU	0004h	B - - -	B A ? ? ? ? ? ?	STU	0006h	- - D C	B A ? ? ? ? D C
ST	0003h	A - - -	A ? ? ? ? ? ? ?	ST	0003h	A - - -	A ? ? ? ? ? ? ?
STU	0005h	- - - B	A ? ? ? ? ? ? B	STU	0007h	- D C B	A ? ? ? ? D C B

FIG. 43

ADD WITH SATURATE			MAXIMUM			TRANSPARENCY		
ADDM	D0, D1, D2		SUBM	D0, D1, D2		CMPM	D0, D1	
MRGM	D2, D3, D2		MRGM	D0, D1, D2		MRGM	D0, D2, D3	
D0 = 89 23 CD 67			D0 = 89 23 CD 67			D0 = 89 23 CD 67		
+D1 = 01 AB 45 EF			-D1 = 01 AB 45 EF			(-)D1 = 23 23 23 23		
D2: = 8A CE 12 56			D2: = 88 67 88 67			(= 66 00 8A 44)		
MFLAGS: = ?? ?? ?? ?3			MFLAGS: = ?? ?? ?? ?5			MFLAGS: = ?? ?? ?? ?4		
D2 = 8A CE 12 56			D0 = 89 23 CD 67			D0 = 89 23 CD 67		
D3 = FF FF FF FF			D1 = 01 AB 45 EF			D2 = 87 65 43 21		
D2: = 8A CE FF FF			D2: = 89 AB CD EF			D3: = 89 65 CD 67		
COLOUR EXPANSION			COLOUR COMPRESSION			GUIDED COPY		
LD	*A0, MFLAGS		CMPM	D0, D1, D2		LD	*A0, MFLAGS	
MRGM	D0, D1, D2					MRGM	D0, D1, D1	
			D0 = 89 23 CD 67					
			(-)D1 = 89 89 89 89					
			(= 00 89 44 CD)					
MFLAGS = XX XX XX X6			MFLAGS = ?? ?? ?? ?8			MFLAGS = XX XX XX XC		
D0 = 11 11 11 11						D0 = 89 23 CD 67		
D1 = 88 88 88 88						D1 = 87 65 43 21		
D2: = 11 88 88 11						D1: = 87 65 CD 67		

FIG. 44

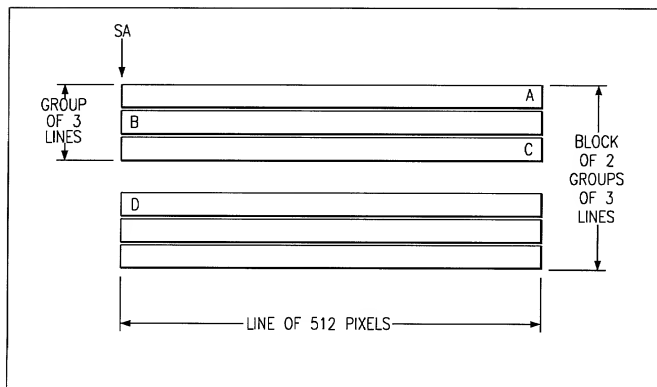
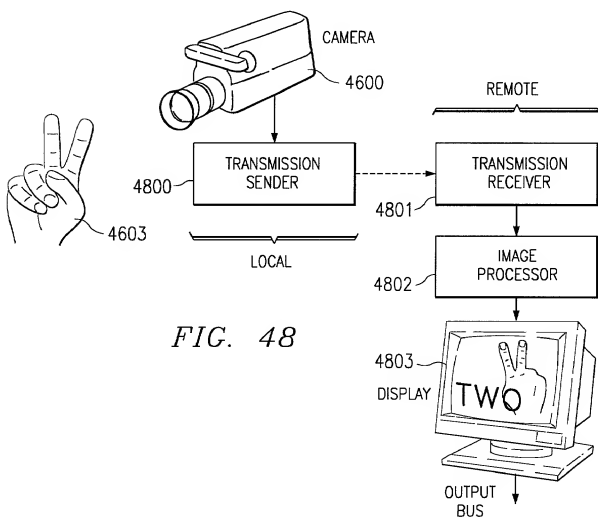
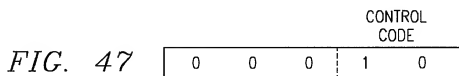
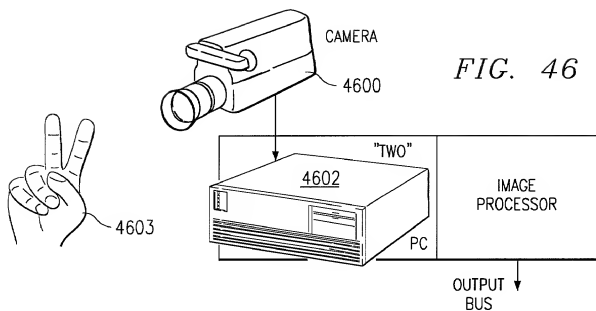
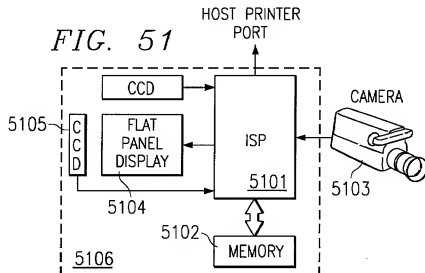
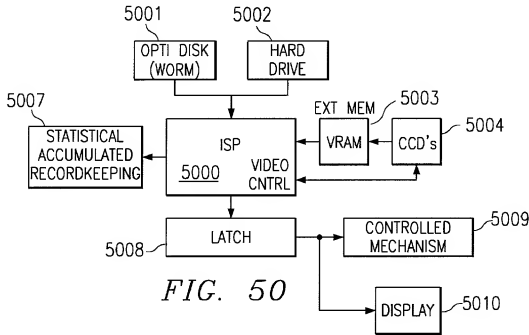
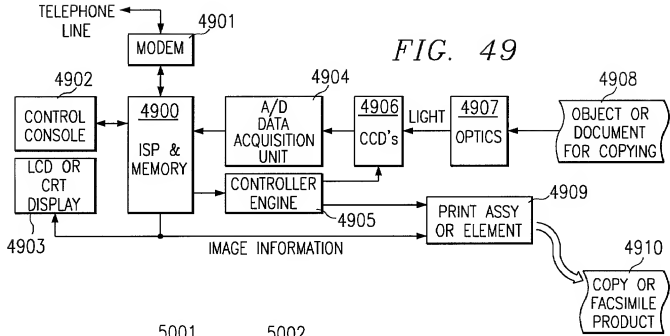


FIG. 45





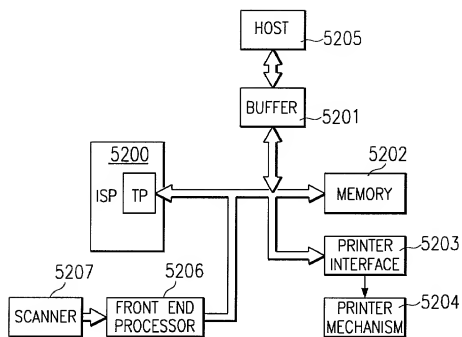


FIG. 52

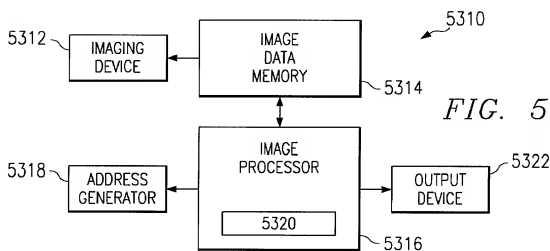
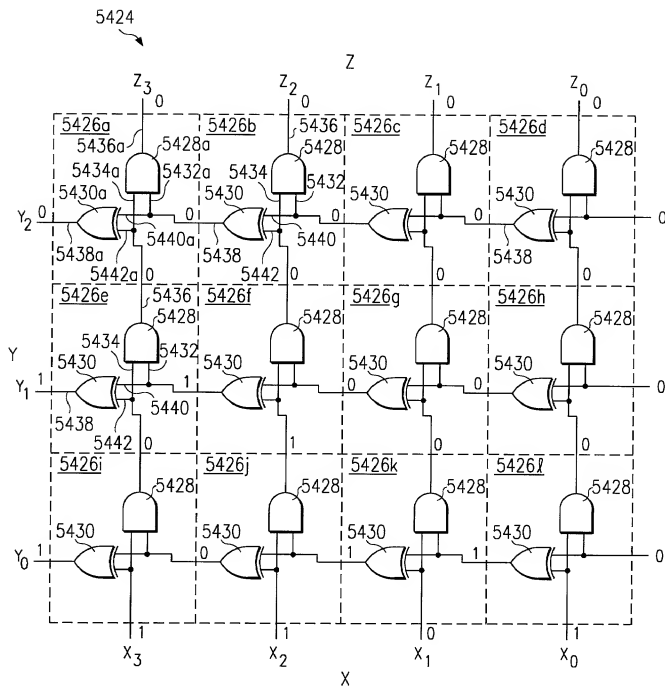


FIG. 53



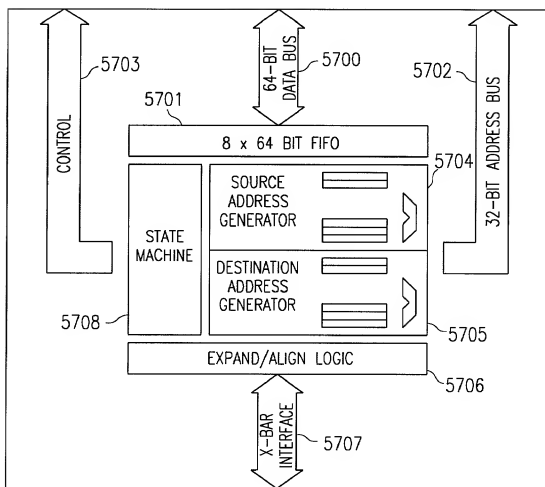


FIG. 57

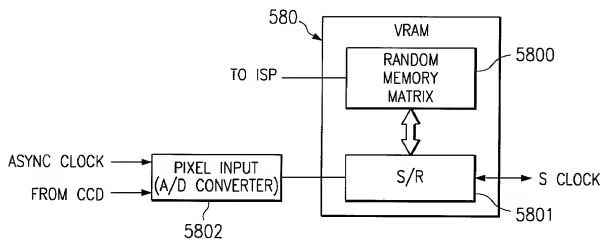


FIG. 58

FIG. 59

(PRIOR ART)

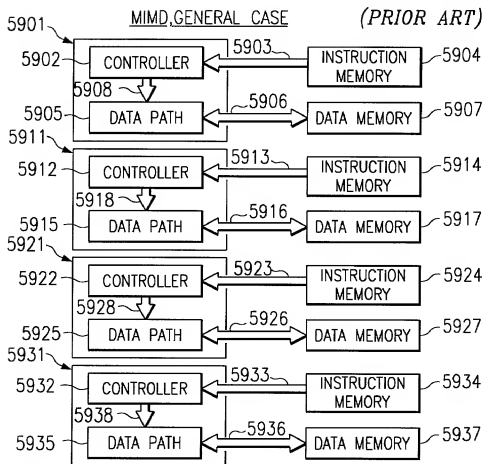


FIG. 60

(PRIOR ART)

